



Japan Patent Office (JP)
Publication of Unexamined Patent Applications (A)

Unexamined Patent Application No. [Kokai Number]: H06(1994)- 45342
Date of Publication of Unexamined Patent Application: February 18, 1994
Request for Examination: Not Requested
Number of Claims: 1
Total pages: 4

<u>Int. Cl. 5</u>	<u>ID Symbol</u>	<u>Internal File Nos.</u>	<u>F1</u>
H 01 L 21/331 29/73		7377-4M	H01L 29/72

RECEIVED
NOV 20 2002
TECHNOLOGY CENTER 2800

(54) Title of Invention: Semiconductor Device

(21) Patent Application No.: H04(1992) -217199
(22) Patent Application Date: July 23, 1992

(71) Applicant 000004237
NEC
5-7-1, Shiba District, Tokyo, Japan

(72) Inventor: Shuji Kanamori
NEC, 5-7-1, Shiba District, Tokyo, Japan

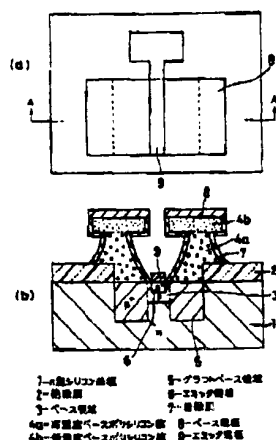
(74) Agent: Yusuke Onomi

Note: Translator's comments are in { }.

Abstract:

[PURPOSE]: To reduce the resistance between the base and the emitter by shortening the distance between the emitter region and a graft base region

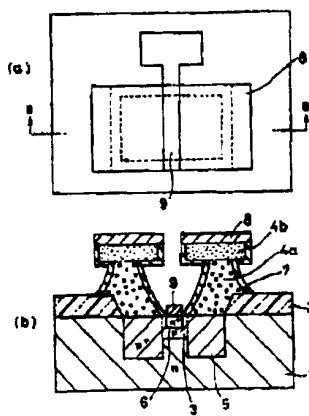
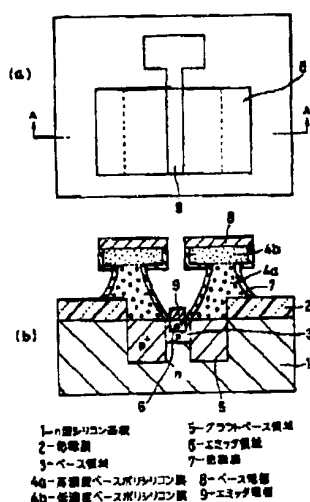
[CONSTITUTION]: A base region (3) is formed in the surface area of an n-type silicon substrate (1), and graft base regions (5) are formed on both sides of it, and an emitter region (6) is formed in the base region (3). The polysilicon film on the graft base region is constituted of a high-concentration base polysilicon film (4a) and a low-concentration base polysilicon film (4b). At patterning of these polysilicon films, the high-concentration polysilicon film is high in etching rate, so the polysilicon film (4a) is side-etched greatly. Ions are implanted into the emitter region, with the photo resist mask used at etching left.



1. N-type silicon substrate
2. Insulator film
3. Base region
- 4a: High-concentration base polysilicon film
- 4b: Low-concentration base polysilicon film
5. Graft base region
6. Emitter region
7. Insulator film
8. Base electrode
9. Emitter electrode

Figure 1

Figure 2



Claims:

[Claim 1]:

The semiconductor device is made as follows: the graft base regions are set around the base region, the polycrystalline silicon film is set on the aforementioned graft base regions, and the emitter region is set on the surface regions on the aforementioned base

regions. It has the configuration characteristics of the aforementioned polycrystalline silicon film made of two parts: the first polycrystalline film being shaped like a prismoid (truncated pyramid) the bottom surface of which touches the base region, and the second polycrystalline film forming a plane-platform shape on top of the first polycrystalline film.

Detailed Explanation of the Invention:

[0001]

Industrial Field of Application:

This invention pertains to a semiconductor device, especially a semiconductor device which includes a high-speed operation bipolar transistor.

[0002]

Prior Art:

Figure 3 shows the cross section of the conventional high-frequency bipolar transistor. The figure shows n-type silicon substrate (1) configuring collector regions, the insulator film (2), p-type base region (3), the high-concentration base polysilicon film (4), the graft base region (5) made of high-concentration p-type region being formed on both sides of base region (3), the emitter region (6a) which is the high-concentration n-type region, the insulator film (7a), the base electrode (8a), the emitter electrode (9a), and high-concentration emitter polysilicon film (10).

[0003]

It is necessary to reduce the resistance between the emitter and the base as much as possible in order to accomplish high speed operation of a transistor. The distance between the emitter region and the graft base region needs to be shortened, which was accomplished by scaling down the size of the transistor or thinning the insulator film (7a).

[0004]

Problem that the Invention Solves:

In the conventional transistor mentioned above, the emitter region (6a) is formed by ion implantation on top of the polysilicon; however, the ion implantation cannot be done for the entire surface of the emitter opening area due to the thick polysilicon film formed around the emitter opening area. Therefore, for instance, when the thickness of the insulator film (7a) is 1000 Å {100 nm} and the polysilicon film (4) thickness is 2000 Å, the distance between the emitter region and the graft base region would be 3000 Å; then the resistance between the base and the emitter would be high.

[0005]

Means of Solving the Problem:

In this invention, the graft base region is configured around the base region, the polycrystalline silicon film is created on top of the graft base region, and the emitter region is configured within the base surface region. Its configuration characteristics of the aforementioned polycrystalline silicon film is that it is made of the first polycrystalline film being shaped like a prismoid (truncated pyramid) the bottom surface

of which touches the base region, and the second polycrystalline film forming a plane-platform shape on top of the first polycrystalline film.

[0006]

Working Example:

This invention is explained using the illustrated working examples. Figure 1 (a) is the plane view of the working example and Figure 1 (b) is its cross section along the A-A line. This semiconductor device in this working example is created as follows. SiO_2 is deposited using CVD method in 1800 Å thickness onto n-type silicon substrate to form the insulator film (2) and transistor formation points are opened on the insulator film (2) using the photo etching method.

[0007]

Base region (3) with the impurity concentration rate of 10^{17}cm^{-3} is formed by implanting boron ions with the insulator film (2) as mask. Subsequently polysilicon is deposited and the boron is implanted to $5 \times 10^{19} \text{cm}^{-3}$ concentration to form the high-concentration layer. Another layer of polysilicon is then grown and implanted with boron ions to 10^{15}cm^{-3} concentration to form the low-concentration layer.

[0008]

The photo resist mask, covering the opening of insulator film (2) excluding the emitter formation region, is formed next. The high-concentration base polysilicon film (4a) and low-concentration base polysilicon film (4b) are formed by etching the polysilicon film in nitric acid etching solution. Due to the difference in etch rate caused by the difference in impurity concentration, high-concentration base polysilicon film (4a) forms the prismatic shape.

[0009]

The emitter region (6) is formed by ion implantation of phosphorous with the aforementioned photo resist mask. After the photo resist mask is removed, the boron in the high-concentration base polysilicon film (4a) is diffused by a thermal process for the formation of the graft base region (5) as well as the low resistance of the low-concentration base polysilicon film (4b).

[0010]

Using CVD method, SiO_2 film is deposited in 1000 Å thickness and the insulator film (7) is formed only on the sides of the base polysilicon film (4a, 4b) using anisotropic dry etching. Al {aluminum} is deposited using an anisotropic ion deposition method. The Al deposited on top of the polysilicon film remains separate from the rest of Al film. On this Al film, photo etching is done to form base electrode (8) and the emitter electrode (9).

[0011]

Figure 2 (a) shows the top plane view of the second working example of this invention. The figure 2 (b) shows its cross section view along the B-B line. The difference from the second* working example is that the insulator film (2) has tapered sides. In order to enable the high-speed transistor, the insulator film (2) needs to be thicker so that the

parasitic capacitance of the emitter electrode {inter-electrode capacitance} is small. When the insulator film becomes more than 2000 Å thick, there is the danger of the emitter electrode breaking at the plane gap. So to prevent this kind of breakage, the electrode has tapered sides in this example.

*{Translator's note: * "...second working example..." seems incorrect, based on the context. The translator believes it should be read "...first working example."}*

[0012]

So far the working examples show the preferred examples but this invention is not limited to these examples and can be modified as needed. For example, the insulator film (2) can be formed via LOCOS method and the polysilicon film (4a, 4b) can be doped at the time of the film formation.

[0013]

The patterning of the polysilicon can be accomplished by using both anisotropic etching and isotropic etching methods. For example, anisotropic etching can be used to a certain point and can then be switched to isotropic etching. This method enables more precise control of the amount of side etching. The transistor shown in the working examples can be an individual part or an element of an IC (integrated circuit). When used in an IC, the embedded layer is configured.

[0014]

Effects of the invention:

In this invention, the distance between the emitter region and the graft base region is determined by the amount of side etching on the base polysilicon film and, for example, the distance can be as small as 1000 Å. Thus the resistance between the emitter and the base can be reduced and the high-speed operation of the transistor can be accomplished. In this invention, the emitter electrode and the base electrode can be formed in self-alignment method and this contributes to the miniaturization of the semiconductor device.

Legends of the Figures used in the working example:

[Figure 1] Top plane view and cross-section view of the first working example of this invention

[Figure 2] Top plane view and cross-section view of the second working example

[Figure 3] The cross section view of the conventional device

Legends of Symbols {in all figures}:

- 1: N-type silicon substrate
- 2: Insulator film
- 3: Base region
- 4, 4a: High-concentration base polysilicon film
- 4b: Low-concentration base polysilicon film
- 5: Graft base region
- 6, 6a: Emitter region
- 7, 7a: Insulator film
- 8, 8a: Base electrode

10: High-concentration emitter polysilicon film

6a-エリツプ電極
7a-接触電極
8a-ベース電極
9a-エリツプ電極
10-高抵抗エリツプ層(シリコン)

8a-エロップ紙
7a-鉛線筒
8a-ベース電筒